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Posting Counts

Show S Numbers

Edit S Numbers

Preferences

Search Results -

Terms	Documents
11 and (mask with (growth adj suppress\$))	0

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Refine Search:

 11 and (mask with (growth adj
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Clear

Search History

Today's Date: 8/28/2001

<u>DB Name</u>	<u>Query</u>	<u>Hit Count</u>	<u>Set Name</u>
DWPI	semiconductor and (light adj emitting) and mask	198	<u>L1</u>
USPT,PGPB,JPAB,EPAB,TDBD	semiconductor and (light adj emitting) and mask	4461	<u>L2</u>
TDBD	12	14	<u>L3</u>
USPT,PGPB,JPAB,EPAB,TDBD	12 and (mask with (growth adj suppress\$))	1	<u>L4</u>
DWPI	11 and (mask with (growth adj suppress\$))	0	<u>L5</u>

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Search Results - Record(s) 1 through 1 of 1 returned.

☐ 1. Document ID: US 4935936 A

L4: Entry 1 of 1

File: USPT

Jun 19, 1990

DOCUMENT-IDENTIFIER: US 4935936 A

TITLE: Semiconductor structure with flared mesa burying layers

ABPL:

A semiconductor structure and methods for making it, for use in opto-electronic devices, employs only MOVPE growth steps. The structure is based on a mesa having substantially non-reentrant sides. To make it, an initial semiconductor structure is produced which comprises a substrate with a mesa thereon, the mesa having a self-aligned, central stripe of metal organic vapour phase growth suppressing material on its uppermost surface. Burying layers are then grown by MOVPE at either side of the mesa, the stripe removed, and covering layers grown over the mesa and adjoining regions of the burying layers. To make an opto-electronic device, a silica window can be formed on the uppermost surface of the covering layers and contacts provided through the window and to the remote face of the substrate. Two methods of making the initial semiconductor structure are described. Devices such as optical detectors and waveguides can be made using methods according to the invention. Particularly importantly, semiconductor lasers which will operate in a single transverse mode can be made.

BSPR:

The present invention relates to semiconductor structures and methods of making them. It finds particular application in the field of opto-electronic devices such as semiconductor lasers, and their manufacture.

BSPR:

A known family of opto-electronic devices has the following central structure: a substrate of semiconductor material having a mesa thereon, with burying layers on either side of the mesa. Such a device is described by O Mikami et al in "1.5 .mu.m GaInAsP/InP Buried Heterostructure Lasers Fabricated by Hybrid Combination of Liquid--and Vapour-Phase Epitaxy", Electronics Letters, 18 (5) (4.3.82) pages 237-239. The word "mesa" in this context is used to describe an upstanding stripe having steep sides and a flat top.

BSPR:

The devices of the family include a p-n junction across which

current flows (the conventional current from p to n) and a waveguide region to which light is confined. The waveguide region may comprise an "active layer" in which electrons and holes combine with the production of photons by radiative recombination. Such an active layer has to relate suitably in band gap and refractive index to the other semiconductor regions of the structure in order to achieve a suitable degree of "confinement" of these processes to the active layer. The layers of material to either side of the waveguide region and in contact with the opposite faces of the waveguide region are known as "confinement layers".

BSPR:

A major field of application of semiconductor optical devices is in optical fibre communications systems. In general, the devices are constructed out of materials whose elemental components are selected from Groups III and V of the Periodic Table. Silica optical fibres as produced in recent years have loss minima at 1.3 μm and 1.55 μm approximately, the latter minimum being the lower. Accordingly, there is an especial need for devices operating in the range from 1.1 to 1.65 μm , especially from 1.3 to 1.6 μm . (These wavelengths, like all the wavelengths herein except where the context indicates otherwise, are in vacuo wavelengths). Semiconductor lasers operating in this region of the infrared usually comprise regions of indium phosphide, InP, and of quaternary materials indium gallium arsenide phosphides, $\text{In}_{1-x}\text{Ga}_x\text{As}_{1-y}\text{P}_y$. By suitable choices of x and y it is possible to lattice-match the various regions while varying the band gaps of the materials. (Band gaps can be determined experimentally by, for example, photoluminescence). Additionally, both indium phosphide and the quaternary materials can be doped to be p- or n-type as desired.

BSPR:

Describing a selected device of the known family, a semiconductor laser, with its mesa uppermost, it has an active layer within the mesa. Electrical contacts are provided to the mesa and on the furthestmost face of the substrate from the mesa. The "confinement" required is provided optically in a vertical direction, by changes in refractive index of the semiconductor material, and both optically and electrically in a horizontal direction by the burying layers. The burying layers act to cause any current flowing between the contacts to flow preferentially through the mesa and therefore through the active layer. In one form, the burying layers may present non-conducting semiconductor junctions to current flow between the contacts in use of the device.

BSPR:

Good electrical confinement is provided if the semiconductor layers between the contacts constitute a p-n junction and the burying layers in combination with the substrate constitute an n-p-n junction when taken in the same direction. In use the burying layers and substrate then comprise a reverse biased semiconductor junction in both directions. Alternatively the burying layers and substrate could present multiple reverse

biased semiconductor junctions in one or both directions.

BSPR:

In the disclosure by O Mikami et al, a method for manufacturing a device with resistive burying layers is described. The layers which will constitute the mesa, comprising InP and quaternary layers, are grown on a semiconductor wafer by LPE, the mesa being produced by chemical etching on either side of a Si.sub.3 N.sub.4 masking stripe. The burying layers, of high-resistivity InP, are then grown by vapour phase epitaxy (VPE) to either side of the mesa. The Si.sub.3 N.sub.4 stripe remains during the VPE growth stage, preventing growth on the upper surface of the mesa itself, and is only subsequently removed.

BSPR:

A method of fabricating buried mesa structure lasers using only low pressure "metalorganic chemical vapour deposition" (LP-MOCVD) epitaxial growth steps is outlined in the following paper: "Very Low Threshold Buried Ridge Structure Lasers Emitting at 1.3 .mu.m Grown by Low Pressure Metalorganic Chemical Vapour Deposition" by M Razeghi et al, Applied Physics Letters, 46 (2) (15.1.85) pages 131-133. (MOCVD is an alternative term for MOVPE.) The method comprises the steps of growing onto an InP substrate, an n-doped InP confinement layer, an undoped GaInAsP active layer, and a p-doped InP layer for avoiding the formation of defects near the active layer during etching. Etching using a mask, the active layer is reduced to a mesa. After removing the mask, the mesa is covered by a p-doped InP layer and a p-doped GaInAs cap layer.

BSPR:

It is an object of the present invention to provide an improved semiconductor structure and methods of manufacture thereof.

BSPR:

According to a first aspect of the present invention there is provided a semiconductor structure comprising a substrate having a mesa thereon, the uppermost layer of the mesa being provided by InP, and the lateral surfaces of the mesa being substantially non-reentrant, said lateral surfaces being buried by burying layers whose uppermost surfaces extend upwards and away from the uppermost surface of the mesa to form a flared groove.

BSPR:

Semiconductor structures according to embodiments of the present invention have the advantage that they can be fabricated using MOVPE for all growth steps while having InP as the material of the uppermost part of the mesa. InP offers particularly good optical and electrical confinement characteristics.

BSPR:

According to a second aspect of the present invention there is provided a method of making a semiconductor structure, which method comprises the steps of:

BSPR:

By making an initial semiconductor structure as above, the stripe of growth suppressing material can be produced so as to be self aligned, and centrally placed on the mesa.

BSPR:

A particularly important application of the present invention is in the production of lasers which will operate in a single transverse mode. These lasers are of major importance in optical communication systems. Such lasers can be produced from semiconductor structures made by the method of the present invention in which the uppermost surface of the mesa is restricted to being not more than 5 .mu.m wide.

BSPU:

(i) depositing a layer of metal organic vapour phase growth suppressing material on a semiconductor wafer having an InP uppermost layer;

BSPU:

(a) forming a mask of resist material on the layer of growth-suppressing material;

BSPU:

(b) etching the layer of growth-suppressing material, using the resist mask, such that the mask is undercut;

BSPU:

(c) reflowing the resist material of the mask so that the portions of the mask which are undercut drop into contact with the semiconductor wafer;

BSPU:

(d) etching the semiconductor wafer using the resist mask to create the mesa; and

BSPU:

(e) removing the mask of resist material.

BSPU:

(f) forming a mask of resist material on the layer of growth-suppressing material;

BSPU:

(g) selectively etching the layer of growth suppressing material by means of the resist mask to form a double layered mask;

BSPU:

(h) etching the semiconductor wafer using the double layered mask to create the mesa; and

BSPU:

(i) removing the mask of resist material,

DRPR:

A single transverse mode semiconductor laser, and methods for

making it, according to embodiments of the present invention will now be described, by way of example only, with reference to the accompanying Figures in which:

DRPR:

FIGS. 2a to 2f show stages in production of an initial semiconductor structure from the wafer of FIG. 1;

DRPR:

FIGS. 3a to 3f show stages in an alternative method of producing the initial semiconductor structure from the wafer of FIG. 1;

DRPR:

FIG. 4 shows a semiconductor structure which comprises the initial semiconductor structure after burying layers have been grown;

DEPR:

Referring to FIG. 2b, Waycoat W43 negative photoresist material is used to form a mask 7 comprising a stripe 5 .mu.m wide which extends in the <110> direction with respect to the wafer 1. The mask 7 is exposed and developed in the normal manner then baked at 150.degree. C. for 45 secs to prevent the resist from lifting during the next step.

DEPR:

Referring to FIG. 2c, the SiO.sub.2 (silica) is etched using the mask 7 by Countdown "silox etch". Etching is isotropic and therefore the photoresist mask 7 is undercut with a 1:1 undercut to depth ratio. By periodic observation with a microscope, the extent of silica remaining under the mask 7, which is transparent, can be determined and etching is continued until a stripe 16 of silica 1 .mu.m wide remains. Only the silica is etched by this etchant, the layer below it not being affected. Immediately after etching the sample is stored in a desiccator at 10.degree. C. for at least half a day to remove occluded water from beneath the undercut resist. If this is not done, and water remains, the edges of the resist may not be uniform after the next processing stage.

DEPR:

Referring to FIG. 2d, in order to seal the 1 .mu.m silica stripe 16, the sample is heated at 150.degree. C. for 5 mins. This causes the stripe of the photoresist mask 7 to soften and flow to the extent that the undercut portions drop onto the semiconductor surface, sealing in the SiO.sub.2 stripe 16 and restoring the effective mask width to approximately 5 .mu.m.

DEPR:

Referring to FIG. 2e, the next stage is to etch a mesa, using the reflowed photoresist as a mask 7'. The quaternary layer of the wafer substrate forms an active layer in the mesa. It can be desirable that the sides of the mesa should be smooth. If this is so, subsequent growth reliability and reproducibility can be enhanced. Further, smooth sides can lead to improved performance in a completed laser. In order to obtain smooth

sides of the mesa, an etchant which will etch the different layers 2, 3, 4, 5 of the double heterostructure wafer, including the active layer, at substantially equal rates should be used. In the present method a 0.2% solution of bromine in methanol at 20.degree. C. is used but other etchants could be used, such as a solution of bromine in acetic acid. This produces a mesa having only a relatively slight shoulder at the level of the active layer 4.

DEPR:

Again, the extent to which the photoresist mask 7' is undercut during etching can be monitored using a microscope. Etching is continued until the uppermost surface 15 of the mesa is in the range from 1.2 .mu.m to 1.5 .mu.m wide. This dimension range is desirable for correct operation of the completed laser.

DEPR:

The use of the resist mask 7' in etching the mesa is thought to produce a tapered mesa because the mask 7' does not adhere strongly to the material of the wafer, in contrast to silica masks. The latter tend to produce mesas with strongly reentrant lateral surfaces. Resist materials other than the photoresist material specified above may also be found satisfactory. However it must be possible to reflow the material of the resist mask 7 so as to seal the silica stripe 16, by heat or otherwise.

DEPR:

Referring to FIG. 2f, after etching of the mesa the photoresist mask 7' is removed. Removal is carried out using Indust-Ri-Chem Lab resist strip J100 and methanol and the silica stripe 16 is left intact. This sample is then cleaned using H.sub.2 SO.sub.4, rinsed in deionised water and blown dry. The sample at this stage represents the initial semiconductor structure onto which the burying layers are grown, and can be described as a substrate having a mesa thereon, a stripe 16 of silica being centrally positioned on the mesa.

DEPR:

Referring to FIGS. 3a to 3f, in an alternative method of making the initial semiconductor structure, again a double heterostructure wafer 1 as shown in FIG. 1 is the starting point. However in this second method the first step is to oxidise the uppermost surface of the wafer to degrade a subsequentt interface with silica growth-suppressing material.

DEPR:

Referring to FIG. 3b, Waycoat negative photoresist material is again used to form a mask 7 comprising a stripe which extends in the <110> direction with respect to the wafer 1. The stripe in this case is less than 5 .mu.m wide, being for instance from 4 to 4.5 .mu.m wide where a mesa of depth 1.5 .mu.m is intended. The mask is then baked as before, prior to etching the silica layer 6.

DEPR:

Referring to FIG. 3c, the silica layer 6 is etched using the

resist mask 7, to create a double layered mask 16, 7.

DEPR:

Referring to FIG. 3d, the mesa is then etched using 0.2% Br/MeOH as before. Etching is carried out for a pre-selected time period so as to achieve the required depth. The result is a mesa supporting the double layered mask 16, 7, the mask overhanging the lateral surfaces of the mesa.

DEPR:

Because the overhanging silica can cause difficulty in later stages of the laser fabrication, it is removed. Firstly the sample is rebaked so as to seal the resist mask 7 to the silica stripe 16 but without any significant change in profile of the resist mask 7. Then the sample is placed in buffered HF for a time sufficient to etch away the overhanging silica from beneath where the silica is exposed.

DEPR:

Referring to FIG. 3e, the result of etching the overhanging silica as above is to reduce the silica stripe 16 to a width slightly less than that of the uppermost surface 15 of the mesa. The side surfaces of the stripe 16 slope outwards towards the resist mask 7. This sloping characteristic is a result of the rebaking step which seals the resist mask 7 to the silica stripe 16, and is advantageous when burying layers are subsequently grown.

DEPR:

Referring to FIG. 3f, after etching of the overhanging silica, the resist mask 7 is again removed using Indust-Ri-Chem lab resist strip J100 and methanol. This leaves a mesa with a stripe 16 of silica on top, the uppermost surface 15 of the mesa being exposed over a narrow distance at each edge.

DEPR:

Although both methods described above for making an initial semiconductor structure, with reference to FIGS. 2a to 2f and 3a to 3f respectively, result in a tapered mesa, it is only necessary that the mesa should have substantially non re-entrant sidewalls. For instance there should not be an overhang of any part of either of the lateral surfaces equal to more than 10% of the width of the uppermost surface 15 of the mesa. Preferably any overhang should not be equal to more than 5% of the width of the uppermost surface 15 of the mesa. If the sidewalls of the mesa overhang to too great an extent then satisfactory burying layers cannot be grown subsequently by MOVPE.

DEPR:

Referring to FIG. 4, the burying layers 8, 9 are grown in two stages onto the initial semiconductor structure: a 0.4 μm Cd doped InP layer 8, p approximately equal to $5 \times 10^{17} \text{ cm}^{-3}$; and a 0.8 μm S doped InP layer 9, n approximately equal to $1 \times 10^{17} \text{ cm}^{-3}$. Growth conditions again are generally as is normal for MOVPE growth but before growth starts, the sample is heated to 650.degree.

C. for 5 mins in the presence of PH.sub.3. This treatment acts to enhance the action of the silica as a MOVPE growth-suppressing material even at stripe widths as low as 1 .mu.m or so.

DEPR:

This final laser structure can be mounted (not shown) on a heat sink by soldering the heat sink to the contact 13, 14 to the window 18. Because of the planar surface 20, the solder need only have a thickness such as to accommodate the steps produced by the contact window 18. Hence the heat sink can be brought into close proximity to the semiconductor material of the mesa.

DEPR:

Devices such as optical detectors or optical waveguides may also be made using methods according to the present invention which is not limited to the production of semiconductor laser.

CLPR:

1. A semiconductor structure comprising:

CLPR:

2. A semiconductor structure according to claim 1 wherein the burying layers consist of material grown by metal organic vapour phase epitaxy and have a shape characteristic of such growth technique.

CLPR:

3. A semiconductor structure according to claim 1 or 2 wherein the mesa tapers substantially along all its lateral surfaces towards its uppermost surface.

CLPR:

4. A semiconductor structure according to claim 1 or 2 wherein the mesa comprises an active layer.

CLPR:

5. A semiconductor structure according to claim 4 wherein the active layer comprises gallium indium arsenide phosphide.

CLPR:

6. A semiconductor structure according to claim 1 or 2 wherein the substrate comprises at least one layer of indium phosphide.

CLPR:

7. A semiconductor structure according to claim 1 or 2 wherein the burying layers comprise indium phosphide.

CLPR:

8. A opto-electronic device comprising a semiconductor structure according to claim 1 or 2 wherein said mesa includes an active light emitting layer.

CLPR:

9. A semiconductor laser comprising a semiconductor structure

according to any one of the preceding claims 1 or 2 wherein said mesa includes an active light emitting layer optically confined to form a resonant lasing cavity.

CLPR:

10. A semiconductor laser device comprising:

CLPR:

11. A semiconductor device comprising:

CLPR:

12. A semiconductor structure comprising:

CLPR:

13. A semiconductor structure comprising:

CLPR:

14. A semiconductor structure as in claim 13, wherein said further burying layer is grown on one of a plurality of intermediate burying layers formed on said first burying layer.

CLPR:

15. A semiconductor structure comprising:

CLPR:

16. A semiconductor structure as in claim 15, wherein said plurality of burying layers comprises only said first and said second burying layer, said second burying layer providing the uppermost surfaces of said plurality.

CLPR:

17. A semiconductor structure comprising:

CLPR:

18. A semiconductor structure according to claims 12, 13 or 15 wherein the burying layers each have a shape characteristic of having been grown by metal organic vapour phase epitaxy.

CLPR:

19. A semiconductor structure according to claims 12, 13, 15 or 17 wherein the lateral surfaces of said mesa tapers towards its uppermost surface.

CLPR:

20. A semiconductor structure according to claim 12, 13, 15 or 17 wherein the mesa comprises an active layer.

CLPR:

21. A semiconductor structure according to claim 20 wherein the active layer comprises gallium indium arsenide phosphide.

CLPR:

22. A semiconductor structure according to claim 12, 13, 15 or 17 wherein the substrate comprises at least one layer of indium phosphide.

CLPR:

23. A semiconductor structure according to claim 12, 13, 15 or 17 wherein the burying layers comprise indium phosphide.

CLPR:

24. A semiconductor structure as in claim 12, 13, 15 or 17 wherein the mesa includes at least one layer capable of performing an opto-electronic function, said structure including electrode means.

CLPR:

25. A semiconductor structure as in claim 12, 13, 15 or 17 wherein the mesa includes at least one layer providing a resonant lasing cavity and wherein said structure includes electrode means.

CLPV:

a semiconductor substrate having a first electrode structure on one side;

CLPV:

a mesa formed on said substrate and having at least three semiconductor layers therein, at least one of such mesa layers being capable of emitting light in response to current passing therethrough and being disposed between other mesa layers having a lower refractive index than the refractive index of the light emitting mesa layer;

CLPV:

a first burying layer of semiconductor disposed on either side of said mesa and substantially covering both lateral side surfaces of the mesa, said first burying layer also having a lower refractive index than that of the light emitting mesa layer;

CLPV:

a second burying layer of semiconductor disposed on top of said first burying layer and extending onto the top lateral edges of the uppermost mesa layer and having uppermost opposed surfaces extending first upwardly and then away from the top surface of the mesa to form a flared groove inside the lateral top surface edges of the mesa;

CLPV:

at least one covering layer of semiconductor extending over said flared groove and said second burying layer, and

Full	Title	CIT.1	REV.1	CLS.1	REF.1	DRAW.1
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Generate Collection

Terms	Documents
l2 and (mask with (growth adj suppress\$))	1

Display

20

Documents, starting with Document:

1

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WEST**Generate Collection****Search Results - Record(s) 1 through 14 of 14 returned.**☐ 1. Document ID: NN960875

L3: Entry 1 of 14

File: TDBD

Aug 1, 1996

DOCUMENT-IDENTIFIER: NN960875

TITLE: Full Color Active Matrix Display Based on GaN Lateral
Light Emitting Diode Structures

TBTI:

Full Color Active Matrix Display Based on GaN Lateral Light
Emitting Diode Structures

TBTX:

This document contains drawings, formulas, and/or symbols that will not appear on line. Request hardcopy from ITIRC for complete article. GaN is a wide bandgap semiconductor capable of emitting light of various colors, dependent on the impurities introduced into the crystal (1). Electroluminescence from GaN Light Emitting Diodes (LEDs), both the p-n junction diode and m-i-n diode variety, has been realized in all of the visible colors (1, 2). Therefore, the potential exists to make a full color display from an array of GaN LEDs in which the active impurity responsible for the emission color is laterally varied.

TBTX:

In addition, a practical display must also be compatible with an inexpensive active matrix technology in order to realize high performance. For example, LCD technology is commonly integrated with Si thin film transistor arrays fabricated on glass. A GaN LED based display would also benefit from an on-board active matrix capability. - We now address a novel lateral LED structure, which when realized in GaN, fulfills the above criteria for GaN LED based display technology. This is to the best of our knowledge, the first realization of a lateral LED structure, and could also find applications in discrete LED or small LED array applications in GaN or other semiconductor systems. Fig. 1 shows the cross section of the simplest embodiment of a lateral GaN LED 10. The lightly shaded region 11 is n-type GaN, which can be doped during epitaxial growth across the whole wafer. The darker shaded region 12 represents the area in which an active impurity has been introduced though some sort of mask. Active impurities in GaN are deep levels, and therefore this region 12 is electrically insulating. This simplest device structure could be improved by the introduction of a dielectric layer between the Schottky contact and the GaN

channel to control leakage current and minimize surface recombination. During operation, electrons are injected from the ohmic contacts 13 into the compensated center region 12 where they recombine radiatively with active impurity sites which dictate the resulting photon color. An important point is that the current injection is symmetric, i.e., from either side, or possibly from all sides (if the active region is circular, the n-type region 11 might be a ring around it). In all cases, light is emitted through the transparent substrate 14, which is typically sapphire.

TBTX:

(2) Compound Semiconductor Magazine, Vol. 1, No. 3 (1995).

Full	Title	Citation	Front	Review	Classification	Date	Reference	Claims	KWIC	Draw	Desc
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☐ 2. Document ID: NN9004397

L3: Entry 2 of 14

File: TDBD

Apr 1, 1990

DOCUMENT-IDENTIFIER: NN9004397

TITLE: Servo Scheme for Patterned Media Using Optical Detection Integrated with the Head Structure.

TBTX:

- Disclosed is the application of optical servo techniques to magnetic recording on patterned media by integrating optics into the slider. Provision is made to precisely align the optical components with conventional heads used to read/write data. - Patterned media formed by etching discrete tracks on the surface of rigid disks have been investigated recently for conventional magnetic recording (1). One potential advantage of this technology is the possibility of achieving high track density by using the patterned tracks as a source of servo information. Many schemes have been proposed for this including capacitance sensing and various servo-on-data schemes, such as center-tapped magnetoresistive heads. It is obvious that optical detection of the patterned tracks is also possible in analogy to optical disks. In fact, there have been proposals to eliminate a bulky focusing mechanism for optical disks by placing the optics on a slider supported by an airbearing using either on-slider optics they_{2,3} or optical fibers to connect to optical components on the arm they₄. One difficulty with applying these proposals to discrete tracks in conventional recording is aligning the optical detectors with the read/write heads. We propose here a scheme which facilitates that alignment. - The invention consists of using lithographically defined optical waveguides to couple light from a light source to the patterned surface of a magnetic disk. The light that is backscattered from the disk reenters the waveguide and a portion of it is directed to one or more optical detectors. The waveguides could be fabricated on the same substrate as the thin film magnetic head using an additional lithographic mask

step. The accuracy of alignment of read/write heads with the optical servo detector will be determined by the limitations of mask alignment. - One possible implementation of the invention is shown in the figure. Light from a semiconductor laser or light-emitting diode is coupled into a waveguide, which might consist of aluminum oxide or other high refractive index dielectric. The light is carried by the waveguide to the air bearing surface of the slider. The light exits the waveguide and illuminates a small portion of the patterned media. Since the air bearing surface of the slider is only a fraction of a wavelength above the disk surface, negligible diffraction occurs and the width of the illuminated area is determined by the waveguide geometry. The size of the illuminated region can be as small as several microns. The lateral displacement of the waveguide from the read/write head is controlled by mask alignment and, in this case, is an integral multiple of the track pitch. - The light emitted by the waveguide strikes the disk surface and part of it is backscattered. The backscattered light reenters the waveguide structure and a portion of it is directed to the two detectors. When the waveguide is centered over the center of the track, the backscattered light will have an angular distribution which is symmetric. When the waveguide is off-track, the backscattered light will have an asymmetrical intensity pattern which is used to generate a tracking error signal by taking the difference between the two detector signals. (This same asymmetry in the reflected light is used in optical disk systems to generate the tracking error signal.) It may be desirable to have more than one optical source with detectors to provide unambiguous servo information. - A related method for generating a tracking error signal is to use the laser itself as a detector via well-known "feedback" effects (3,5). For example, a laser operated near threshold will generate substantially more light in the presence of feedback light than in the absence. This increase in light output can be detected with a photodiode located behind the laser, as described in (3). Alternatively, one can take advantage of the change in current-voltage (I-V) characteristics of the diode which depends on the level of the feedback light. In particular, the presence or absence of feedback light can be detected by measuring the voltage across the diode when the diode is driven with constant current (5). - SUMMARY This disclosure proposes to use integrated optical techniques to generate the tracking error servo signal for recording on patterned magnetic media. Waveguides are used to channel the light to and from the disk surface. The waveguides are accurately aligned with respect to the magnetic head using photolithographic techniques. - References (1) S. E. Lambert, I. L. Sanders, A. M. Patlach, and M. T. Krounbi, "Recording Characteristics of Submicron Discrete Magnetic Tracks," IEEE Trans . Mag . 23, 3690 (1987). (2) K. Itao and S. Hara, "High Performance Optical Disk Storage System," Jpn . J . Appl . Phys . 26, 177 (1987). (3) H. Ukita, Y. Katagiri, and Y. Uenishi, "Readout Characteristics of Micro-optical Head Operated in Bi-stable Mode," Jpn . J . Appl . Phys . 26, 111 (1987). (4) N. Koshino and S. Ogawa, "Optical Method of the Head Positioning in Magnetic Disk Systems," IEEE Trans . Mag . 16, 631 (1980); F.S. Barnes, K.S. Lee, and A.W. Smith, "Use of Optical Fiber

Heads for Optical Disks," Appl . Opt . 25, 4010 (1986). (5) Y. Mitsuhashi, T. Morikawa, K. Sakurai, A. Seko and J. Shimada, "Self-coupled Optical Pickup," Opt . Commun . 17, 95 (1976).

Full	Title	Citation	Front	Review	Classification	Date	Reference
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KWIC	Draw. Desc
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☐ 3. Document ID: NN830655

L3: Entry 3 of 14

File: TDBD

Jun 1, 1983

DOCUMENT-IDENTIFIER: NN830655

TITLE: Laser Marking Using Latching AMPLIFIER PELS Which Are Light-Activated Silicon-Controlled Rectifiers Made of Amorphous Silicon

TBTX:

- Prior media for laser marking required almost all the energy density to be delivered during the very brief dwell time per picture element (pel). Both amplification and pulse stretching are needed in the medium itself. - Laser liquid crystal displays and laser videodisk recorders and similar devices use a brief laser flash to mark a medium. These systems are limited by the briefness and power of the flash. This light- activated latching electrical amplifier is arranged with many small amplifier pels, each covering one dot of the display. These are electrically or thermally coupled to an adjacent display or recording stratum. The amplifiers are constructed from 4 semiconductor layers which are doped PNP and form light-activated silicon-controlled rectifiers (LSCRs). A favorable fabrication is to gas deposit hydrogenated amorphous silicon (a-Si:H) with codeposited doping. This can be done over large areas, and requires only one masking process, and no critical alignment. - In operation, a voltage is applied across the amplifying stratum, but little current density flows before illumination. A brief light flash can turn on a LSCR pel, which then latches into a conducting state. Thus, each pel amplifies and remembers the presence or absence of a flash until it is reset by reducing the applied voltage. By subdividing the electrodes which supply this voltage, there can be simultaneous marking, storing and erasing in different zones. - Background In laser marking systems, an economical diode laser has limited power to mark rapidly on a stable recording layer. Two examples are videodisk recorders (VDRs) and laser addressed liquid crystal displays (LLCDs). One approach is to develop a more powerful laser and a better recording medium with lower writing energy density. Another approach is to add amplification in the medium itself. - An initial amplification attempt was to add a photoconductive amorphous hydrogenated silicon layer (PC a-Si:H) to a field-effect liquid crystal (LC) display. Voltage is applied across the PC and LC layers in series, but without the laser illumination the large PC resistance blocks the voltage from appearing across the LC. A laser flash makes the PC pel resistance drop, and voltage appears across the LC which

causes a visible phase transition. However, the laser pulse is only about 20 microseconds long, and the LC transition requires voltage for about a millisecond. Although the photoconductivity persists after the laser pulse, it is still too brief for a practical system. - A second amplifying system uses PC and a thermally switched LC. Voltage is applied across only the PC layer. When the laser illuminates a pel, the resulting photoconductivity causes fast local ohmic heating which is thermally conducted slowly into the LC and causes a transition. Although the LC response time is no longer critical, it is difficult to deposit enough energy density during the brief conductive interval. - These systems, and many other laser addressed marking systems, need a planar photo-electric latching amplifier. Ideally, a brief light pulse triggers a sustained effect, so a conveniently small power density (or voltage or current density) is applied to the display layer for a conveniently long time. This latching amplifier switches a large voltage and a large current density. It gives a large power density and energy density amplification for brief light pulses. It has a large contrast between on and off states. Finally, it is readily fabricated in a cell with many pels. - A third amplifying system uses standard crystalline semiconductor techniques to make an IC with one photo-electric amplifier and one memory cell per pel. There are fabrication and cost problems. A display typically requires on the order of a million pels. Therefore, crystalline defect density and lithography quality are critical. - The preceding systems had different virtues. The PC a-SiH system showed the fabrication advantages of an amorphous semiconductor and a simple pel structure. The crystalline IC systems showed the flexibility of transistor-style electronics. - LSCR The present latching amplifier stratum consists of many pel-sized light-activated silicon-controlled rectifiers. One can be triggered by a brief light flash of limited intensity. Then it conducts as long as an electrical voltage is applied. The SCR structure switches a large voltage and a high current density. It has a large contrast ratio between on and off conductivity (or current density or voltage). A planar SCR gives amplification and memory with only 4 uniform layers, and does not depend on mask-produced structure. However, the pels may be separated by a more defined etching process if pel "blooming" is a problem. - Although an SCR is usually considered a DC latch, AC latching should also be achievable. An SCR will not unlatch if its DC supply is interrupted very briefly because of the finite carrier recombination time. Make a symmetrical PNP structure, which can latch in either direction. Trigger symmetrically by using a light whose absorption length exceeds the LSCR thickness. When powered by AC, this device is latched securely when either polarity voltage is applied. Only during the transitions through zero voltage is there any possibility to unlatch. Therefore, a frequency is used whose transition time is too fast to permit substantial recombination. - There are many slightly different SCR-like structures: triacs, diacs, silicon-controlled switches, etc. Also, electrodes could form a layer by forming a Schottky barrier with the semiconductor. Any device which uses a PNP structure for latching amplification or any planar latching amplifier is used. Large LSCRs have

previously been made from crystalline semiconductors for power switching. One can start with such a device, mount it in a display cell, then divide it into many pel-sized subunits. - Amorphous Silicon An alternative embodiment uses amorphous silicon. Start with a transparent substrate covered with a transparent electrode. Use an RF discharge to apply four successive layers of hydrogenated amorphous silicon which are doped by codeposited gas additives to form a PNP SCR structure. Passivate the top surface and add an electrically conducting, optically reflecting layer. Apply a lithographic mask and etch this large SCR structure into many small SCR pels, each covering one dot in the display. Fill the grooves with an opaque electrical insulator. (This structure is appropriate for electrically coupling to a reflectively projected display stratum.) Slightly different structures are appropriate for thermal coupling or for transmission projection optics. - This embodiment has certain advantages. A-Si:H can be uniformly deposited over the several square centimeters required for a typical projection display cell. (Considering the active work towards practical a-Si:H solar cells, even larger areas may become feasible.) In addition, since the doping is codeposited with the a-Si:H itself, it will be uniform through the thickness of each layer, and very thin layers can be made. This helps make bipolar amplification feasible. By comparison, crystalline devices are feasibly made by diffusing a dopant into a crystal slice. Layer thinness and uniformity are limited by the exponential profile of the dopant concentration. (Some epitaxially grown crystalline semiconductors can also be doped by codeposition, with corresponding advantages.) Switching Externally switching the overall voltage can have several useful effects. To minimize the effects of leakage currents, switch the voltage on just before the flash. If the display medium has its own memory, the LSCR can produce the mark and soon be turned off. If the display medium lacks memory, then the voltage is sustained so the LSCR latch is the main memory. In that case, the display is erased by switching off the voltage. - These external switching processes can be applied to the whole cell, or applied to a selected zone. Divide the front and back electrodes into X and Y strips, respectively. To apply full voltage selectively, turn on one X and one Y strip. To turn off selectively, apply full voltage to all but one X and one Y strip. (The half-selected row and column will have half voltage which should keep their LSCRs latched.) A more complex external switching system combines zonal selective activation and erasing. Suppose that marking and erasing required voltage of $\pm 2V$, and $\pm V/2$, respectively. Normally, maintain all strips at $\pm V$. Selectively change one X strip and Y strip to $\pm V/2$. - FEASIBILITY AND APPLICATION NOTES CONCERNING a-Si:H LSCR AMPLIFIER PELS Application Example: Projected Color TV These latching amplifier displays have many applications. As a reference point, we compare this system with a standard TV signal. Then follows a more serious, systematic discussion of applications. Assume that the data order and timing are flexible, and not predefined by a standard TV signal. (This assumption helps show the new capabilities, but it is not critical.) Because of the latching amplification, we may be able to use a light-emitting

diode (LED) as the marking light source. Then, we could use the large LED arrays being developed for xerographic printing. Thus, a light bar of 1000 LEDs and lenses is practical. Therefore, the optical raster scanning system is simplified, by eliminating the fast horizontal scan, to leave only the slow vertical scan. Suppose a LSCR pel triggers in 1 msec and resets in 10 msec. Use zonal switching to reset 10 old lines just ahead of the line being marked. Thus, erasing does not affect the writing rate. A frame of 1000 columns by 1000 rows can be marked by the light bar in 1 msec. Even at this rate, each pel is available for display for more than 98 percent of the time. This latching amplifier display can show: .IN 0 1000 columns x 1000 rows x 1 bits/sec x 1000 frames/sec = 109 bits/sec compared to a standard color TV signal: .IN 0 500 columns x 5000 rows x 12 bits/pel x 30 frames/sec = 0.9 x 10⁷ bits/sec where: 12 bits/pel = 3 colors x 4 intensity bits/color pel To make a TV display, the design could trade frames/sec for bits/ pel. For example, modulate the overall projection light among 3 colors and 4 binary-spaced intensity levels in a cycle of 12 binary frames per shaded color TV frame. Since the display overlaps successive binary frames as it sweeps the light bar across the display, the modulator should also overlap successive frames in

Full	Title	Citation	Front	Review	Classification	Date	Reference
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KWIC	Draw Desc
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☐ 4. Document ID: NN78112562

L3: Entry 4 of 14

File: TDBD

Nov 1, 1978

DOCUMENT-IDENTIFIER: NN78112562

TITLE: Solid State Multiple Electron Gun for Improved Display Cathode Ray Tube. November 1978.

TBTX:

3p. An improved cathode ray tube (CRT) is provided for information display with potential for high resolution and brightness together with lower flicker through the use of multiple electron streams in parallel. - The cathode ray tube is a useful device for information display. It is possible to make a very satisfactory low-cost display terminal with screen content up to about 4000 characters using raster scan technique. Although such terminal involves a number of technical compromises, it works remarkably well, has good reliability, and has provided the basis for extremely rapid growth of the display terminal market. - These displays use a raster-scan CRT chassis similar to the TV equivalent (either monochrome or color), and large-scale integration (LSI) digital circuitry to provide a local character buffer, character generation memory (read-only memory or random-access memory), and video timing generation. For handling keyboard, display, and communications control, a microprocessor may be used to provide flexible, featurable control. Such displays can easily have 500 to perhaps 4000 characters, color (with somewhat

reduced quality), and limited graphics. - With up to perhaps 1000 raster lines and refresh rates in the 25-60 hertz range, CRT displays based upon raster scan are both low cost and easy to implement. Beyond that level, difficulties rise rapidly. These difficulties include problems with brightness, deflection power, and data rate. With modern components, electron-beam resolution is not a problem. Thus, CRT displays capable of 10,000 raster lines are achievable, but not at frame rates or brightness suitable for human viewing. - The limits of CRTs for displays are all associated with the serial nature of the device. The brightness limit comes from the brightness achievable from reasonable, long-life electron guns and the requirement that the single gun be time-multiplexed over the entire screen. The more spots addressed on the screen, the more the multiplexing, and the lower the brightness of any one spot. The data rate and deflection power limits are associated with the need to keep frame rates high enough that flicker is not a serious problem, which ranges approximately from 25 to 60 hertz depending upon the application, use of interlace, and phosphor persistence. - The picture element (pel) time is just $1/\text{frame rate} \times \text{pels per frame}$. The pel time is a controlling factor in the gain bandwidth requirement for the final video amplifier, and sets the speed required on the character buffer and character generator memories. Pel times under 50 nanoseconds are achievable, but at high cost and with unsatisfactory brightness. - The horizontal scan frequency which equals the frame rate \times the scan lines per frame is a major element in determining the required power for the deflection circuits. The power required goes up approximately as the square of the horizontal scan frequency, and the cost of deflection goes up faster than the required power. - An integrated multiple electron gun is proposed here which is capable of producing close-spaced but independently controlled electron streams. Enough electron streams are created (7-40) to write a whole line of characters in one sweep across the screen. This would reduce the horizontal scan frequency by roughly the degree of parallelism, as well as increase the pel time by the same amount. This advantage could be used to provide increased screen content, freedom from flicker and better brightness. The parallelism has favorable impact on character generation. This is done with a memory having a parallel output which must be serialized for conventional CRTs. Parallel electron streams also reduce the speed requirements for the character buffer random-access memory. - This solid-state multicathode is based upon a combination of semi-conductor light-emitting-diodes (LEDs) which have an integral photo-cathode on their surface. The light from the LEDs causes emission of electrons from the photocathode which is used as the electron source in a field-limited electron gun structure. One common electron acceleration and lens structure is used for a row of LED/photocathode emitters to make a row of independently controlled electron streams. - Typical electron-beam currents used in conventional CRT displays are on the order of 50 to 100 microamps. In this multi-beam system, these might be reduced by an order of magnitude. Since permissible currents for a LED with a good heat-sink are on the order of 0.5 amps, a conversion efficiency from electrons into the LED to electrons

emitted into the vacuum of 0.0001 or better is probably necessary. This conversion efficiency can be achieved either of two ways. One is to use a direct-gap semiconductor for the LED, such as GaAs. Such LEDs can have efficiencies as high as 0.1 (particularly into a photocathode material of similar index of refraction). The light from these LEDs will excite common near-infrared cathode materials. These materials have a quantum efficiency in the neighborhood of 0.01. It is also possible that the GaAs or equivalent semiconductor with an appropriate low electron affinity coating can operate as its own photocathode. - The second approach is to use an indirect-gap semiconductor, such as GaP, for the LED. Recent progress in LEDs of these materials has resulted in quantum efficiencies approaching 0.01. These LEDs have their output in the yellow, green, or blue where very good photocathodes exist with quantum efficiencies of 0.1 to 0.2. While this approach would probably not give enough brightness for a single-gun conventional CRT, it appears adequate for the multi-gun case. - An advantage of this system is that the drive voltages needed for the LEDs are low, even though they are relatively high current. This requirement is much easier to fill in a logic environment than the high-voltage requirement for conventional CRTs. Another feature of this multi-beam approach is that it is applicable to slot-mask type color by using three rows of LED/photocathodes which are focussed and converged together on the screen. Although slot-mask color is presently inferior to triad (dot-mask) color, advances in etching of the tube shadow-mask could change this.

Full	Title	Citation	Front	Review	Classification	Date	Reference
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☐ 5. Document ID: NN77033959

L3: Entry 5 of 14

File: TDBD

Mar 1, 1977

DOCUMENT-IDENTIFIER: NN77033959

TITLE: Merging Semiconductor Optoelectronics With Silicon Technology. March 1977.

TBTI:

Merging Semiconductor Optoelectronics With Silicon Technology. March 1977.

TBTX:

2p. This article proposes an approach for mounting an independently processed GaP LED (light-emitting diode) array on a silicon carrier on which all the necessary electronics and interconnection patterns are prefabricated. The connections between the array and carrier are then made to form an integrated system. - Figs. 1 and 2 illustrate a preferred approach to achieve this result, although several variations may be used to accomplish the same result. - As shown in Fig. 1, the fabrication of LED array 1 incorporates the standard highly efficient GaP LED technology using such steps as: liquid or vapor-phase deposition of GaAsP layer 2 on GaP substrate 3; Zn-diffusion through a mask to form P-diffused regions 4; and the introduction of isoelectronic traps either as atomic (N) or molecular traps (Zn-O) to achieve the efficient radiative transitions at room temperature. Beam-lead technology is used on LED array 1 to act both as contacts 5 and 6 to the individual P region 4 and n layer 2, respectively, as well as the bridge between GaP array 1 and the silicon carrier, as shown in Fig. 2. At the bottom of GaP substrate 3, a partially reflecting region 7 and absorbing region 8 in the form of an electrically nonconducting coating, are employed, so the light, in the case of region 7, is reflected and re-emitted from the top of the devices of array 1 and, in the case of region 8, light is absorbed to provide the optical isolation necessary between the LED diodes. - Referring now to Fig. 2, silicon carrier 10 has a channel 11 etched away on one side thereof to accommodate the LED array 1. All the necessary electronics, interconnections and contacts to the LED beam-lead contacts 5 and 6 are fabricated by the standard silicon planar process. LED array 1 is then glued or just placed in channel 11 with its surface aligned with the surface of carrier 10. Beam-lead contacts 5 and 6 are then soldered to contacts 12 on silicon carrier 10. The integration of the total system is thus completed. - From the above description it should be clear that channel 11 in silicon carrier 10 is not a necessary step, if a planar structure is not required. The beam-lead approach provides the necessary flexibility to bridge the contacts at two different surface levels. Other kinds of semiconductor optoelectronics material, such as GaAs, can be utilized in the way described to achieve system integration. - The above approach is particularly advantageous in that it provides the most straightforward and simple way to implement an integrated system which incorporates two different technologies. Also, it preserves the features of both technologies without compromise.

Full	Title	Citation	Front	Review	Classification	Date	Reference
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KWIC	Draw. Desc
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☐ 6. Document ID: NN74033200

L3: Entry 6 of 14

File: TDBD

Mar 1, 1974

DOCUMENT-IDENTIFIER: NN74033200

TITLE: Fabrication for Light Emitting Diode Array. March 1974.

TBTI:

Fabrication for Light Emitting Diode Array. March 1974.

TBTX:

1p. This technique is used to form a light-emitting diode (LED) X-Y array on a monolithic substrate. - A mask in combination with a photolithographic and etching process is used to form parallel elongated rows (corresponding to one axis of the array) of spaced elevated regions (plateaus), on the upper surface of an epitaxial layer of a given conductivity type. The epitaxial layer is previously grown on a semiconductor substrate. The plateaus are used to support the LEDs of the array, which are subsequently formed thereon by a vapor epitaxy system. - The mask is provided with a spatial periodicity, e.g., 5 microns, that allows the subsequent formation of the PN diode layer exclusively on the surfaces of the parallel elevated regions (plateaus), but prevents or inhibits the formation of the PN layer on the surfaces of the lower regions (valleys) which are located between the elevated regions. Thus, the resultant elongated parallel spaced rows of the diode layer are electrically isolated from each other. The etching process step which would otherwise be required to provide this isolation is thus eliminated. B Next, the rows of the diode layer are divided along the other axis of the array to form the individual diodes. To this end, electrical isolation in the transverse direction is provided by using conventional masking, photolithing and etching techniques. As a result, an X-Y monolithic array of diodes is formed. - To provide the electrodes for the diodes, the bottom surface of the substrate, which is also the bottom surface of the assembly, is provided with a contiguous metallization layer to form a common electrode. On the upper surface of the assembly, the interstices between the isolated diodes are filled with a layer of material such as SiO(2) such as for example by RF sputtering. A subsequent lapping of the upper surface of the SiO(2) layer is provided so that the upper P or N (as the case might be) regions of the diodes are exposed. An X-Y transparent conductor pattern with an intersection over each so exposed diode region is formed on the upper surface of the assembly. A "1/2 select" voltage technique is applied to the X-Y conductors in coaction with the bottom common conductive layer, to select the appropriate diode of the array for emission. - Using the foregoing techniques, a matching detector array can be similarly fabricated. The detector array and LED array when aligned form a high-density package or large-scale integrated

aligned form a high-density package or large-scale integrated optical coupling device.

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☐ 7. Document ID: NN73081018

L3: Entry 7 of 14

File: TDBD

Aug 1, 1973

DOCUMENT-IDENTIFIER: NN73081018

TITLE: Integrated Semiconductor LED Display Panel. August 1973.

TBTI:

Integrated Semiconductor LED Display Panel. August 1973.

TBTX:

2p. Integrated semiconductors have successfully replaced all the vacuum tubes in display systems such as a television receiver, for example, except for the cathode-ray tube. The described technique provides a light-emitting diode (LED) display panel, complete with memory cells and the requisite selection circuitry and accessing circuitry on a single monolithic substrate, using basic silicon processing. Small regions of gallium phosphide are selectively grown on silicon or on sapphire, enabling the entire display array to be placed on the same macrochip that also contains all of the required silicon support circuitry. - In many cases, a display panel is situated at a remote location with respect to the source of signals actuating the display. It is desirable to provide the panel with sufficient memory to store the picture formed by a given pattern of energized light-emitting diodes, in order to reduce the data rate in the communication channel between the display and the source of data signals. Low-data rate is facilitated by eliminating the need for constantly regenerating the nonchanging information. The memory stores the nonchanging information and maintains the corresponding portion of the visual display. It is further desirable that all of the required semiconductor circuitry from the logic to the display element be integrated on one monolithic substrate, to obviate the interconnection problem associated with driving the light-emitting elements from a separate semiconductor support chip. - Monolithic semiconductor chips are "flip-chip" mounted on a glass substrate. Viewing is accomplished through the glass to the active side of the chip. The array of light-emitting diodes, respective memory cells and the associated accessing circuits are formed on the active side of the chip. Each light-emitting diode is driven by a respective memory cell such as a flip-flop, so that the diode is energized when the cell is in a first condition and de-energized when the cell is in its opposite condition. An entire panel may consist of 128K illuminatable spots LED arranged as a 256 by 512 spot array, for example. The spots are continuous, in order that graphics as well as alphanumeric characters can be displayed anywhere on

the panel. - Each set of drivers is used to access a different row or column of LED memory cells. Adequate space is available between the illuminatable spots for integrating the cells, drivers and wiring. - Bipolar or field-effect transistor (FET) memory cell and accessing circuit configurations may be used on the monolithic chips comprising the display array. Fig. 1 shows a typical structure integrating a gallium phosphide light-emitting diode and bipolar transistor on the same silicon substrate. Fig. 2 exemplifies a field-effect transistor and gallium phosphide light emitting diode integrated on the same sapphire substrate. Of course, field-effect transistors may also be formed on the silicon substrate of Fig. 1 and bipolar transistors may also be formed on the sapphire substrate of Fig. 2. - Referring to Fig. 1, the bipolar device comprising N+ subcollector 1, P base diffusion 2 and N+ emitter diffusion 3 are formed in a conventional manner, in an N epitaxial layer 4 deposited on P/-/ substrate 5. P+ isolation diffusions such as 6 and 7 also are provided. At this point, pockets are etched into the silicon epitaxy with an appropriate mask in the areas to be occupied by light-emitting diodes. The etching is continued until the buried N+ region 8 is reached. Regions 8 and 1 are formed at the same time, then, a III-V light-emitting compound such as gallium phosphide is epitaxially grown on the N+ silicon buried region 8. First, N and then P type gallium phosphide are selectively grown at relatively low temperatures into the pocket, to form the light-emitting diode. Metallization then can proceed in a normal fashion for both the bipolar and the LED devices. - In the alternative structure of Fig. 2, a sapphire substrate 9 is used in lieu of silicon. Silicon is epitaxially grown on a sapphire substrate in areas where FET devices are desired, and the devices are formed in the usual manner. Gallium phosphide then is epitaxially deposited on the sapphire substrate 9, by first depositing P and then N type gallium phosphide at relatively low temperatures to form the LED.

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☐ 8. Document ID: NN7208951

L3: Entry 8 of 14

File: TDBD

Aug 1, 1972

DOCUMENT-IDENTIFIER: NN7208951

TITLE: Integrated Light Emitting PNP and NPN Devices. August 1972.

TBTI:

Integrated Light Emitting PNP and NPN Devices. August 1972.

TBTX:

2p. Figs. 1A-1C illustrate the method by which npn and pnpn structures are made using both diffusion and liquid phase epitaxy (LPE). In Fig. 1A, an n-type substrate 10 is comprised of $\text{GaAs}(y)\text{P}(1-y)$. P-type regions 12 are diffused into the top surface of the substrate, through openings in oxide mask 14. P-type regions 12 are conveniently formed by diffusion of zinc. This forms a pn light-emitting diode array. - After this, another oxide film 16 is deposited on the top surface of substrate 10 and windows are provided therein to expose p-type regions 12. N-type layers 18 of $\text{Al}(x)\text{Ga}(1-x)\text{As}(1)\text{P}(1-y)$ are then grown through the openings in oxide 16. This forms an npn structure, as indicated in Fig. 1B. - In Fig. 1C, a pnpn structure is provided by growing additional layers 20 of p-type $\text{Al}(x)\text{Ga}(1-x)\text{As}(y)\text{P}(1-y)$ by liquid phase epitaxy on n-type layers 18. - This same technique can be used to provide active devices, such as bipolar or field-effect transistor (FET) devices, in III-V semiconductors and alloys. For instance, n-type layers 18 will comprise the emitters or gates of such devices. Thus, n-type regions can be prepared in a planar monolithic environment. For instance, an n-type substrate of a III-V semiconductor such as GaAs can have shallow p-type regions diffused into one surface of the substrate. If a second masking layer is used and a small opening etched into it to expose the diffused p-type region, an emitter of GaAs can be grown by liquid phase epitaxy onto the exposed portion of the p-type base region. The n-type emitter is grown on top of the p-type base region with a minimum of melt-back taking place. Consequently, the emitter is formed without any sidewall capacitance. The emitter can contain aluminum so that its band gap will be larger than that of the p-type GaAs base region. This will form a heterojunction to aid the injection of carriers from the emitter to the base, thus improving device performance.

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☐ 9. Document ID: NN7206180

L3: Entry 9 of 14

File: TDBD

Jun 1, 1972

DOCUMENT-IDENTIFIER: NN7206180

TITLE: Source Shaping in the Fabrication of Semiconductor Light Emitting Diodes by Molecular Beam Epitaxy. June 1972.

TBTI:

Source Shaping in the Fabrication of Semiconductor Light Emitting Diodes by Molecular Beam Epitaxy. June 1972.

TBTX:

2p. The performance of immersed semiconductor photo-sources depends on effects such as absorption and total internal reflection. The photometric figures of merit in terms of efficiency, radiance, or radiance intensity, therefore, are strongly dependent on the source geometry. A specific shape of geometry would result in a specific optimum figure of merit required for different applications such as display, data retrieval and optically-coupled microcircuits. For example, a hemispherical source would give a maximum efficiency; while a paraboloidal source, a maximum radiant intensity. - In conventional methods, desirable geometries are difficult to achieve, and usually a number of processing steps are involved including cutting, lapping, and etching. A simplified technique for source shaping by the incorporation of a movable mask during the process of growing the material by evaporation is as follows: Fig. 1 shows schematically the pertinent parts of an apparatus for molecular beam evaporation. Included are a source, a substrate and a holed mask movable along the z-direction. Additional sources and masks can be added if required. By moving the mask toward the substrate, the area of deposition reduces. The final shape of the material grown is determined by the time-dependence of the mask movement. For example, assuming a constant rate of growth, a linear dependence would result in a cone, and a quadratic dependence, a paraboloid. Other shapes can also be achieved including those which are truncated. Typical materials for evaporation are GaAlAs or other compound and alloyed semiconductors. Source shaping can also be achieved by moving either the source or the substrate or in combination with the mask. The rate of growth, in this case, then, is an additional parameter that can be varied and controlled. - Fig. 2 shows the result of a single photo-source with the N-type semiconductor grown in a hemispherical geometry. The actual photogeneration in this case, is assumed to be a PN light-emitting diode located at the center of the base. The P-region can either be pre-embedded or created during the evaporation by a technique employing a separate dopant source and a patterned mask, as disclosed in an earlier publication (IBM Technical Disclosure Bulletin, Vol.14, No. 11, Pages 3476 and 3477, entitled "Formation of Embedded Components in Semiconductors During Molecular Beam Evaporation," by L. L. Chang and L. Esaki). - In fact, by combining the present technique with the earlier one, arrays or matrices of photo-sources together with electrical connections can be fabricated simultaneously. Fig. 3 shows one example. Semi-insulating semiconductor is used as the substrate. In Fig. 3, cross stripes of P- and N-type semiconductors are first evaporated. The hemispheres can either be the same semi-insulating material as the substrate, or a matched insulator such as silicon oxide or nitride. Fig. 3A shows a cross-sectional view of one of the devices of the array of Fig.

3. Alternatively, as shown in Fig. 4, pedestal p-regions are formed together with the semi-insulating material. The hemisphere can then just be the N-semiconductor. In this case, an insulator film can still be overlaid, if desired, to improve partial internal reflection and passivation.

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KWIC	Draw Desc
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☐ 10. Document ID: NN72053701

L3: Entry 10 of 14

File: TDBD

May 1, 1972

DOCUMENT-IDENTIFIER: NN72053701

TITLE: Memory Systems Utilizing Light Emitting Diodes and Photodetectors. May 1972.

TBTI:

Memory Systems Utilizing Light Emitting Diodes and Photodetectors. May 1972.

TBTX:

2p. A dense monolithic memory chip is provided by combining light-emitting diodes and photodetectors, fabricated together and included in a single module package. The memory may be either of the read-write type or the read-only type, and may be either volatile or nonvolatile, depending on the fabrication technique employed. - A first system, shown in Figs. 1A and 1B, uses photo-silicon-controlled rectifiers or thyristors as detector and memory elements and light-emitting diodes for the light energy source. In Fig. 1A, a chip 1 is formed with light-emitting diodes 2 and silicon-controlled rectifiers 3 spaced laterally therefrom. Appropriate masking may be employed to prevent adjacent cell cross talk. In Fig. 1B there is shown a vertical stacked arrangement which may achieve greater density. The chip 4 is formed with light-emitting diodes 5 adjacent its lower surface. Photosilicon-controlled rectifiers 6 are provided in alignment with diodes 5 and along the upper surface of chip 4. - The light-emitting diodes 2,5 are addressed and the photo-silicon-controlled rectifiers 3,6 respond to the light radiation from diodes 2,5 and latch up to hold the information. By accessing the silicon-controlled rectifiers 3,6 the retained information is available until it is necessary to write again. To erase or reset the silicon-controlled rectifiers 3,6 a clock pulse may be used to remove the latch up voltages and rebias the array. The photo-silicon-controlled rectifiers 3,6 provide latched output levels thereby minimizing detector circuitry. - Figs. 2A and 2B show a second memory system wherein photodiodes are utilized as the accessed sense elements, with a film or crystal layer for the memory element, and light-emitting diodes for the light source. In Fig. 2A, the chip 7 comprises a semiconductor layer 8 having formed adjacent its upper surface, an array of light-emitting diodes 10 and photodiodes 11. Superimposed on

the layer 8 is a memory element 9 having on its upper surface an array of reflective and nonreflective areas, whereby light emitted from a selected pattern of light-emitting diodes 10 may be transmitted upwardly to a reflective area and then downwardly to a respective adjacent photodiode 11, as indicated by the dashed lines. - Reflective memory element 9 may be formed by vacuum deposition on the chip 7. A mask may be utilized to provide the desired memory pattern. - In Fig. 2B, the chip 12 comprises a lower semiconductor layer 13 and an upper semiconductor layer 14 having sandwiched therebetween, a memory element in the form of a film 15 having an array of transparent and opaque areas, each in alignment between a respective light-emitting diode 16 formed in the layer 13 and an aligned photodiode 17 formed in the layer 14. - A third system is shown in Fig. 3, where chip 18 comprises a bulk photodetector in the form of an upper layer 19 superimposed over an intermediate layer 20 constituting the memory element, which may be in the form of a film or crystal. A lower semiconductor layer 21 is formed with an array of light-emitting diodes 22. Memory element 20 may be formed with a photographic emulsion exposed and developed to provide the desired light-transmitting pattern. Memory element 20 may also be formed by a crystalline structure polarized to pass or reject light in the desired areas.

Full	Title	Citation	Front	Review	Classification	Date	Reference
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KWIC	Draw Desc
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☐ 11. Document ID: NN70111419

L3: Entry 11 of 14

File: TDBD

Nov 1, 1970

DOCUMENT-IDENTIFIER: NN70111419

TITLE: Fabricating Light Emitting Diodes. November 1970.

TBTI:

Fabricating Light Emitting Diodes. November 1970.

TBTX:

1p. This process uses a doped oxide as a diffusion source and a transparent electrical contact in the fabrication of a light emitting diode. Light emitting diodes requires a configuration which permits the radiation to escape from the semiconductor in the most efficient way, thus minimizing internal losses. It is therefore desirable to reduce or completely eliminate large nontransparent contact areas (such as metal contacts). This can be done by diffusing Sn as an N dopant into GaAs which leaves the diffused region transparent. If the final contact is also transparent the entire junction area can be utilized for emission. - As indicated in A, an SiO(2) mask 10 is deposited on a P-type GaAs or GaAlAs substrate 12, and a window 14 formed therein. Window 14 defines the configuration of the diode array in the final structure. Layer 16 consisting of a SiO(2) layer heavily doped with Sn is then deposited by the decomposition of a film of polysiloxane mixed with Sn, as shown in B. The Sn-glass layer is applied by spinning or spraying the siloxane polymer over the entire surface of the wafer 12 and heating. Layer 16 is shaped to the desired configuration and heated to form diffused region 18, as shown in C. A final metal lead 20 is made to the tin glass terminal 22. In D there is shown a top view of the individual light emitting diode. The tin glass layer 16 forms the transparent electrical contact and also serves as a diffusion source for forming region 18.

Full	Title	Citation	Front	Review	Classification	Date	Reference
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KWIC	Draw Desc
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☐ 12. Document ID: NN70091028

L3: Entry 12 of 14

File: TDBD

Sep 1, 1970

DOCUMENT-IDENTIFIER: NN70091028

TITLE: Aligning and Inspecting Microelectronic Circuits.
September 1970.

TBTX:

1p. This is an arrangement for precisely aligning successive exposures on semiconductor wafers and for inspecting any desired portion of a wafer surface. The artwork for the first masking operation is provided with as many alignment marks as there are masking operations. The artwork for subsequent masking operations is designed with only one alignment mark for each masking operation. The latter subsequent alignment marks

are projected onto the wafer and are each aligned relative to one of the alignment marks of the first masking operation. - The alignment marks 1, drawing A, are located near the periphery of a mask 2. Light from an emitting source, i.e., a 1000 watt mercury lamp 3 passes through mask 2 containing the desired artwork and alignment marks 1 into a reduction lens 4 which forms the electronic circuits and alignment marks on the photosensitive surface of a semiconductor wafer, i.e., silicon wafer 5. A pair of dual closed circuit Plumbicons 6 together with an optical relay system pick up the specularly reflected light from the wafer surface. While plumbicons have some characteristics that make them preferred over vicicons, both vicicons and orthocons can also be used. Thus, small mirrors 7 on each side of wafer 5 direct light from two small areas near the periphery of the wafer. Images on these areas are subsequently amplified by the relay lenses 8 before reaching the Plumbicon system. The mirrors 7, when properly adjusted, do not obstruct the wafer area and during exposure, the area receives the same amount of light as the rest of the wafer. The latter result is achieved by choosing a proper exit angle for the principal ray for a given lens numerical aperture. - During the alignment process, alignment filters 9 are introduced between light source 3 and the condenser lens to prevent the overall exposure of the wafer surface. Alignment filters 9 contain only two small apertures and suitably comprises neutral density and glass filters such as those designated as Wratten #39 glass filters. The function of the filters is to eliminate the green and yellow spectrum lines which are also transmitted by a 4047 angstroms interference filter. The Wratten #39 filter is used because some 4047 angstroms interference filters are not blocked sufficiently at all wavelengths. Consequently, Plumbicons 6 receive only the 4047 angstroms light. Exposures of about 30 seconds during alignment do not produce any effects on the photoresist on wafer 5. All information relayed to Plumbicons 6 is then displayed on monitor screens 10, which are suitably connected to the system. - In B, there is illustrated the appearance of the alignment marks on monitor screen 10. The diamond shaped alignment mark 12 is etched on the wafer and mark 13 is the projected real image from mask 9. By wafer manipulation, alignment marks 12 and 13 may be aligned with each other. When using the arrangement for inspecting purposes, wafer 5 is placed on an x-y table and traversed under the light path to permit any single segment on the wafer to be displayed on monitor screens 10. Circuits having from one to five-micron line widths and amplified 200 times would readily display any breaks in the circuit to enable rapid acceptance or rejection of any single segment.

Full	Title	Citation	Front	Review	Classification	Date	Reference
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KWIC	Drawl Desc
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☐ 13. Document ID: NN70041870

L3: Entry 13 of 14

File: TDBD

Apr 1, 1970

DOCUMENT-IDENTIFIER: NN70041870
TITLE: Image Converter. April 1970.

TBTX:

2p. The structure for converting input infrared images to visible images employs varying band-gap GaAlAs structures of the type shown in A and B. Semiconductor 10 has a central n region and two end p regions which form pn junctions. The material is formed during growth so that the band gap at the left or input end is essentially that of GaAs and, therefore, input infrared light is absorbed. The bias voltage reverse biases the junction at this end of the device to normally prevent current flow through the device, but the absorbed infrared provides hole electron pairs and a photocurrent flows, therefore allowing current flow across the forward biased junction at the other end. The forward biased junction acts as a light-emitting diode whose output is in the visible range. - Many such diodes can be made and connected in parallel as shown in C and D. These diodes are fabricated from a wafer of material having the band-gap variation in B which is diffused with p dopants on both sides. Contacts are evaporated through a mask to form a large circular contact to the wide-band gap side, and an array of 1 mil diameter dots to the other side as shown in the top row of C. A thin wire saw is used to cut slots in two dimensions to a depth as indicated in D and spaced as shown in C. This creates an array of diodes having a density of 40,000 per in/2/. A wire bonder is used to connect all the squares in parallel. - A lens system is used to focus an image of 1.4 ev light onto the 1.4 ev array. Photocurrent, proportional to the intensity of illumination, flows only in those diodes illuminated. Due to the mechanical isolation, these spots of current also flow in the corresponding 2.0 ev junction in isolated areas. An eyepiece is used to view the resultant visible image formed on the 2.0 ev face. Since many squares per inch can be made, high resolution results. Also, since only enough voltage is required to forward and reverse bias two junctions, a low voltage of less than 5 volts is sufficient. Since virtually no current flows except when photocurrent is induced, a low drain is taken from the battery.

Full	Title	Citation	Front	Review	Classification	Date	Reference
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☐ 14. Document ID: NN66041569

L3: Entry 14 of 14

File: TDBD

Apr 1, 1966

DOCUMENT-IDENTIFIER: NN66041569

TITLE: Electroluminescent Display. April 1966.

TBTX:

2p. The display is formed of a plurality of electroluminescent diodes arranged in thirteen positions represented by blocks 10 in A. Each position of the matrix includes one diode 12 for each numeral to be displayed. All diodes 12 for each numeral are connected to an input terminal T to which a signal is applied when the numeral is to be displayed. - Only connections for displaying numerals 1...4 are shown and therefore certain of the diodes 12 are not used but these diodes can be used and other diodes added to display other numerals. Diodes 12 need not be grouped in locations but can be formed of a plurality of rows with connections made to a different group of diodes for each character to be displayed. The structure is fabricated out of a single semiconductor wafer with the electroluminescent junctions and interconnections to form the individual characters being made by diffusion through masks. The light emitting junctions can be formed in character segments rather than the dot type diodes shown with the segment junctions for each character being formed by diffusion through appropriate masks. - As in the case of the dot type structure, each segment is used for one character and no decoding circuitry is required. Insulating layers are required between metallic connections to the diodes at crossover points but the character segments themselves are arranged so as not to intersect each other. The integrated structure can also be fabricated by first forming a large planar junction in a semiconductor substrate and then etching selectively to form either the desired dot or segment patterns or both.

Full	Title	Citation	Front	Review	Classification	Date	Reference
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Generate Collection

Terms	Documents
12	14

Display

20

Documents, starting with Document:

14

Display Format:

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Change Format
